AMENDMENTS TO CLAIMS

• Please amend pending claims 1, 4, 5, 6, and 7 as indicated below. A complete listing of all claims and their status in the application are as follows:

1. (currently amended) A clock doubler comprising:

clock doubling circuitry for generating from a system clock an output clock signal having a frequency substantially double that of the system clock and also having a pulse width and associated duty cycle;

timing circuitry for generating a first signal indicative of the time the output clock signal is low, and a second signal indicative of the time the output clock signal is high

comparison circuitry for comparing the first signal and the second signal; pulse width varying circuitry for varying the pulse width of the output clock signal based on the result of comparing the first signal and the second signal; and

a tap delay line connected to receive at least the first signal ~~for delaying the system clock~~, wherein:

the timing circuitry ~~generates a signal by tracking~~ tracks the delay ~~of the clock signal~~ through the tap delay line; and

the ~~output~~first signal ~~of the timing circuitry~~ is indicative of the delay through the tap delay line.

2. (original) The clock doubler as claimed in claim 1 wherein:

the clock doubling circuitry comprises a clock splitter.

3. (canceled)

4. (currently amended) The clock doubler as claimed in claim 1, further comprising:

~~a first tap delay line for delaying the first signal;~~

a second tap delay line for delaying the second signal, wherein:

the comparison circuitry uses a comparator, the comparator comprising:

a first input indicative of the delay through the first tap delay line;

a second input indicative of the delay through the second tap delay line; and

outputs indicative of whether the first signal is greater than, less than, or equal to the second signal.

5. (currently amended) The clock doubler as claimed in claim 1, further comprising:

variable delay chain circuitry for controllably varying the delay of the output clock signal.

6. (currently amended) The clock doubler as claimed in claim 1, further comprising:

delay chain circuitry for controllably delaying the output clock signal, wherein:

the pulse width varying circuitry varies the delay of the output clock signal through the delay chain circuitry.

7. (currently amended) The clock doubler as claimed in claim 1, further comprising:

delay chain circuitry for varying the delay of the output clock signal;

delay control circuitry for controllably varying the length of the delay chain; and

phase determining circuitry for determining the amount of time the output clock signal is high and the time the output clock signal is low.

8. (original) A clock doubler for varying a system clock to generate a second clock signal comprising:

a clock splitter having a first output indicative of the time the second clock signal is low and a second output indicative of the time the second clock signal is high;

a first tap delay line connected to receive the first output and having a first tap delay output;

a second tap delay line connected to receive the second output and having a second tap delay output;

a comparator connected to receive:

the first tap delay line output as a first comparator input;

the second tap delay line output as a second comparator input; and

a comparator output indicative of whether the first comparator input is greater than, less than, or equal to the second comparator input; and

whereby the time the second clock signal is low or high is variably controlled by the comparator output.

9. (original) The clock doubler as claimed in claim 8, wherein the clock splitter comprises:

a delay chain having variably controlled length;

a delay control for variably controlling the length of the delay chain; and

logic circuitry for tracking the time the second clock signal is low and tracking the time the second clock signal is high.

10. (original) The clock doubler as claimed in claim 8 wherein the clock splitter comprises:

a delay chain having a variably controlled length of delay chain elements; and

a delay control for selecting a specific delay chain element in the delay chain.

11. (original) The clock doubler as claimed in claim 8, wherein:

the first tap delay line and the second tap delay line each comprises:

a number of tap delay cells connected to delay the propagation of the first output through the tap delay cells.

12. (original) The clock doubler as claimed in claim 8, wherein the comparator comprises:

a subtractor for performing a subtraction function on the value of the first output and the value of the second output; and

a function generator connected to the subtractor for generating the comparator output.

13. (original) The clock doubler as claimed in claim 8 further comprising:

a register having an input connected to the first tap delay line output; and

a register output connected to the first comparator input.

14. (original) The clock doubler as claimed in claim 8 wherein:

the comparator output is indicative of incrementing the time the second clock signal is low if the first output of the clock splitter is greater than the second output of the clock splitter; and

the comparator output is indicative of decrementing the time the second clock signal is low if the first output of the clock splitter is less than the second output of the clock splitter.

15. (previously presented) A method of correcting the duty cycle of a clock doubler comprising:

generating from a system clock a clock signal having a frequency substantially double that of the system clock and also having a pulse width and associated duty cycle;

generating a first signal indicative of the time the clock signal is low;

generating a second signal indicative of the time the clock signal is high

comparing the first signal and the second signal; varying the pulse width of the clock signal base on the result of comparing the first signal and the second signal;

generating the first signal and generating the second signal generates a signal by tracking the delay through a tap delay line; and

the magnitude of the tracking signal is indicative of the delay through the tap delay line.

16. (original) The method of correcting the duty cycle of a clock doubler as claimed in claim 15 wherein:

generating a clock signal uses a clock splitter.

17. (canceled)

18. (original) The method of correcting the duty cycle of a clock doubler as claimed in claim 15 wherein comparing the first signal and the second signal uses a comparator:

having a first input indicative of the delay through the tap delay line of the first signal;

having a second input indicative of the delay through the tap delay line of the second signal; and

having outputs indicative of whether the first signal is greater than, less than, or equal to the second signal.

19. (original) The method of correcting the duty cycle of a clock doubler as claimed in claim 15 wherein:

varying the pulse width of the clock signal varies the delay of the clock signal through a delay chain.

20. (original) The method of correcting the duty cycle of a clock doubler as claimed in claim 15 wherein:

varying the pulse width of the clock signal increments the time the clock signal is low if the first signal is greater than the second signal; and

decrements the time the clock signal is low if the first signal is less than the second signal.

21. (previously presented) A clock doubler comprising:

clock doubling circuitry for generating from a system clock a clock signal having a frequency substantially double that of the system clock and also having a pulse width and associated duty cycle;

timing circuitry for generating a first signal indicative of the time the clock signal is low, and a second signal indicative of the time the clock signal is high

comparison circuitry for comparing the first signal and the second signal;

pulse width varying circuitry for varying the pulse width of the clock signal based on the result of comparing the first signal and the second signal; and

a first tap delay line for delaying the first signal;

a second tap delay line for delaying the second signal, wherein:

the comparison circuitry uses a comparator, the comparator comprising:

a first input indicative of the delay through the first tap delay line;

a second input indicative of the delay through the second tap delay line; and

outputs indicative of whether the first signal is greater than, less than, or equal to the second signal.

22. (previously presented) A clock doubler comprising:

clock doubling circuitry for generating from a system clock a clock signal having a frequency substantially double that of the system clock and also having a pulse width and associated duty cycle;

timing circuitry for generating a first signal indicative of the time the clock signal is low, and a second signal indicative of the time the clock signal is high

comparison circuitry for comparing the first signal and the second signal; pulse width varying circuitry for varying the pulse width of the clock signal based on the result of comparing the first signal and the second signal;

delay chain circuitry for varying the delay of the clock signal;

delay control circuitry for controllably varying the length of the delay chain; and

phase determining circuitry for determining the amount of time the clock signal is high and the time the clock signal is low.

23. (previously presented) A method of correcting the duty cycle of a clock doubler comprising:

generating from a system clock a clock signal having a frequency substantially double that of the system clock and also having a pulse width and associated duty cycle;

generating a first signal indicative of the time the clock signal is low;

generating a second signal indicative of the time the clock signal is high

comparing the first signal and the second signal; and

varying the pulse width of the clock signal base on the result of comparing the first signal and the second signal;

wherein comparing the first signal and the second signal uses a comparator:

having a first input indicative of the delay through the tap delay line of the first signal;

having a second input indicative of the delay through the tap delay line of the second signal; and

having outputs indicative of whether the first signal is greater than, less than, or equal to the second signal.